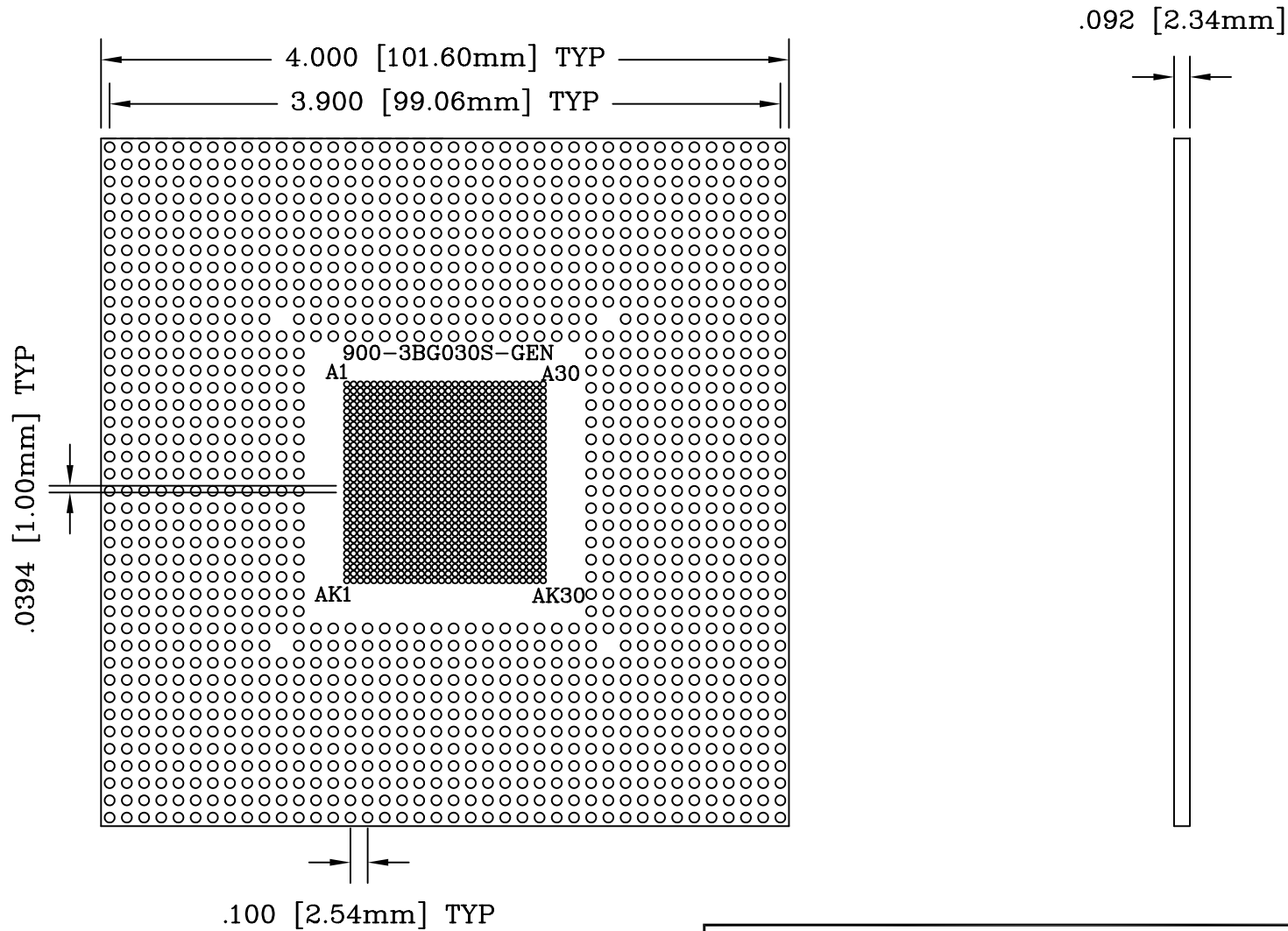
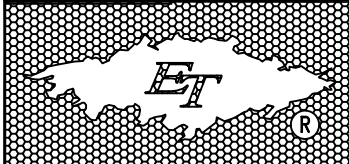


REV	DESCRIPTION	DATE	BY
A	NEW DRAWING	04/21/05	H.N.
B	UPDATED PG 2 PIN OUT	11/19/07	JAG
C	CORRECTED PIN MAP	08/27/09	JAG

F7020



ALL DIMENSIONS ARE IN INCHES UNLESS OTHERWISE SPECIFIED



Emulation Technology, Inc.
 — VLSI and SMT ADAPTERS and ACCESSORIES —

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 CAMARILLO, CA 93012

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SHEET: 1 OF 2	DATE: 04/21/05	REVISION: C	ASSEMBLY DRAWING
CHECKED: Perry Munroe	DRAWN: Huy Nguyen	ITEM: 900-3BG030S-GEN	
Scale 1:1	DO NOT SCALE DRAWING		DESCRIPTION: 900-3BG030S-GEN



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ITEM: 900-3BG030S-GEN
DESCRIPTION: 900-3BG030S-GEN

DATE: 8/27/2009
REVISION: C

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PIN MAP for 900-3BG030S-GEN

Table with 36 columns and 40 rows showing pin connections for the 900-3BG030S-GEN device. The table lists various pins (GND, G7, F7, etc.) and their corresponding connections across the device's pins.