

16M x72, 32M x72, 64M x72, 128M x72 Registered ECC SDRAM DIMM

Registered ECC SDRAM DIMM Based on 16M x4, 32M x4, 64M x4, 4Banks, 3.3V SDRAM's with SPD

GENERAL DESCRIPTION

These Legacy devices are JEDEC standard 16/32/64/128 x72, high density registered synchronous memory modules. These Legacy devices consist of eighteen or thirty-six CMOS 16Mx4, 32Mx4, 64Mx4, 4 bank synchronous DRAM's in TSOP 400-mil packages on a 168-pin glass epoxy substrate, utilizing the Canopy™ 3-D chip carrier technology on dual banked versions. One 0.µF and one 0.33µF decoupling capacitors are mounted on the circuit board and Canopy™ in parallel for each SDRAM. The 128M/256M/512M/1024M devices are Dual In-line Memory Modules and are intended for mounting in 168-pin edge connector sockets.

Synchronous design allows precise cycle control with the use of system clock. I/O transactions are possible on every clock cycle. Range operating frequencies, programmable latencies allows the same device to be useful for a variety of high bandwidth, high performance memory system applications.

FEATURES

- Performance Range 133MHz 7.5ns
125MHz 8ns
- Supports 133MHz or 100MHz bus
- Registered inputs with one-clock delay
- Phase-lock loop (PLL) clock driver to reduce loading
- JEDEC standard ECC pinout in a 168-pin dual in-line memory module (DIMM)
- Single +3.3V ± 0.3V power supply
- LVTTTL compatible inputs and outputs
- Fully synchronous, all signals registered on positive edge of PLL clock.
- Internal pipelined operation, column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Auto & Self Refresh capability
- Serial Presence Detect with E²PROM (SPD)
- 6 layer PCB.

Max Freq. (Speed)

Pin Configurations (Front Side/Back Side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	V _{SS}	29	DQM1	57	DQ18	85	V _{SS}	113	DQM5	141	DQ50
2	DQ0	30	CS0#	58	DQ19	86	DQ32	114	CS1#	142	DQ51
3	DQ1	31	NC	59	V _{DD}	87	DQ33	115	RAS#	143	V _{DD}
4	DQ2	32	V _{SS}	60	DQ20	88	DQ34	116	V _{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V _{DD}	34	A2	62	NC	90	V _{DD}	118	A3	146	NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V _{SS}	92	DQ37	120	A7	148	V _{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V _{SS}	40	V _{DD}	68	V _{SS}	96	V _{SS}	124	V _{DD}	152	V _{SS}
13	DQ9	41	V _{DD}	69	DQ24	97	DQ41	125	•CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V _{SS}	71	DQ26	99	DQ43	127	V _{SS}	155	DQ58
16	DQ12	44	NC	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	CS2#	73	V _{DD}	101	DQ45	129	CS3#	157	V _{DD}
18	V _{DD}	46	DQM2	74	DQ28	102	V _{DD}	130	DQM6	158	DQ60
19	DQ14	47	DQM3	75	DQ29	103	DQ46	131	DQM7	159	DQ61
20	DQ15	48	NC	76	DQ30	104	DQ47	132	•A13	160	DQ62
21	CB0	49	V _{DD}	77	DQ31	105	CB4	133	V _{DD}	161	DQ63
22	CB1	50	NC	78	V _{SS}	106	CB5	134	NC	162	V _{SS}
23	V _{SS}	51	NC	79	•CK2	107	V _{SS}	135	NC	163	•CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V _{DD}	54	V _{SS}	82	SDA	110	V _{DD}	138	V _{SS}	166	SA1
27	WE#	55	DQ16	83	SCL	111	CAS#	139	DQ48	167	SA2
28	DQM0	56	DQ17	84	V _{DD}	112	DQM4	140	DQ49	168	V _{DD}

Ordering Info:

- 36x6BSBR-1yAG (128Meg)
- 37x6ESBR-1yAG (256Meg)
- 38x6JSBR-1yAG (512Meg)
- 39x6JSBR-1yAG (1024Meg)

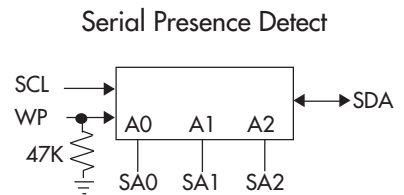
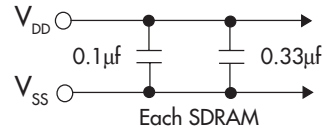
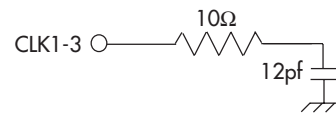
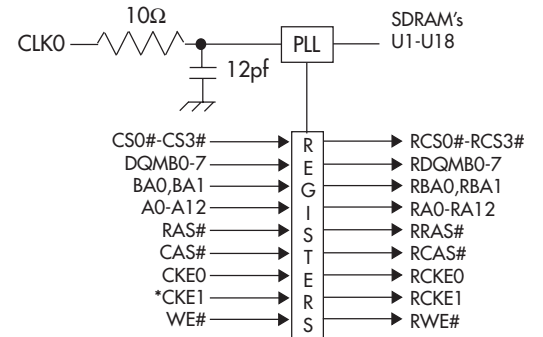
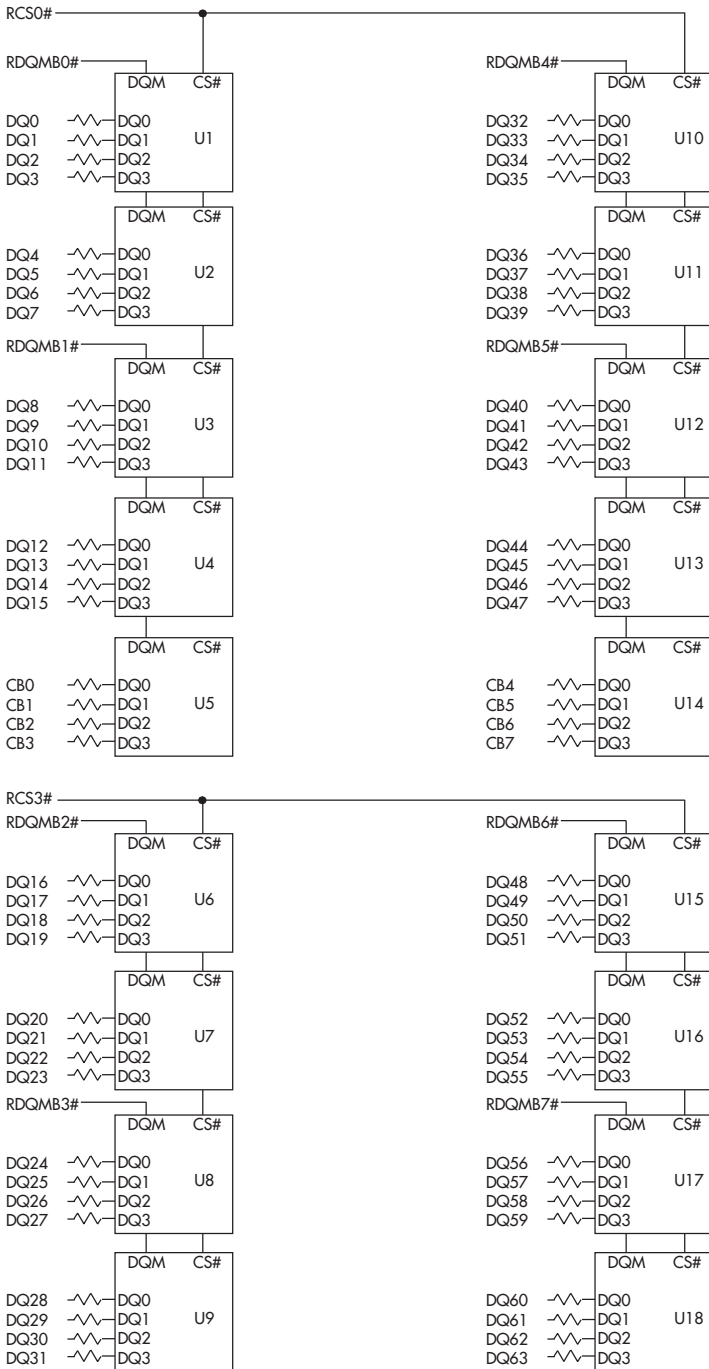
- x = DRAM Supplier
L = Legacy
M = Micron
- y = Height
B = 1.6"
A = 1.7"
0 = 1.7" (obsolete)
- z = Timing
E = PC100 CL2
H = PC133 CL3
G = PC133 CL2

•These pins are not used in this module

Pin Descriptions

PIN	Name	Input Function
CK	System Clock	Active on the positive going edge to sample all inputs.
CS#	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE, and DQM.
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to the new command. Disable input buffers for power down in standby. CKE should be enabled 1CLK+tss prior to valid command.
A0 ~ A12	Address	Row / Column addresses are multiplexed on the same pins. Row address: RA0 ~ RA11, column address: CA0 ~ CA9 (16Mx4) RA0 ~ RA11, column address: CA0 ~ CA9, CA11 (32Mx4) RA0 ~ RA12, column address: CA0 ~ CA10 (64Mx4)
BA0 ~ BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank to be activated during read/write column address latch time.
RAS#	Row Address Strobe	Latches the row addresses on the positive going edge of the CLK with RAS low.
CAS#	Column Address Strobe	Latches the row addresses on the positive going edge of the CLK with CAS low. Enables column access.
WE#	Write Enable	Enables write operation and row precharge. Latches data in starting from CAS, WE active.
DQM0 ~ 7	Data Input / Output Mask	Makes data output Hi-Z, Tshz after the clock and masks the output. Blocks data input when DQM active. (Byte masking)
REGE	Register Enable	The device operates in the transparent mode when REGE is low. When REGE is high, the device operates in the registered mode. In registered mode, the Address and control inputs are latched if CLK is held at a high or low logic level. The inputs are stored in the latch/flip-flop on the rising edge of CLK. REGE is tied to VDD through 10K ohm resistor on the PCB. So if REGE of the module is floating, this module will be operated as registered mode.
DQ0 ~ 63	Data Input / Output	Data inputs/outputs are multiplexed on the same pins.
CB0 - CB7	Check Bit	Used on ECC modules.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
NC	No Connection	N/A

Functional Block Diagram

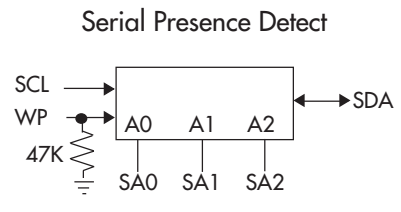
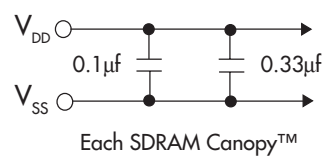
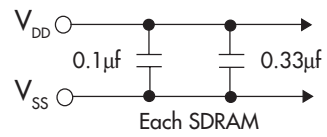
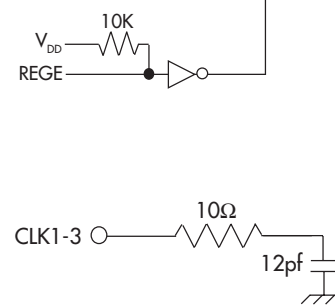
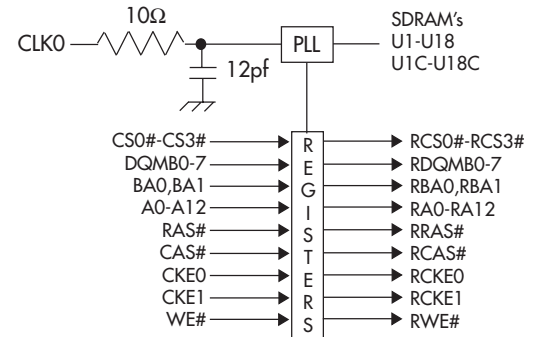
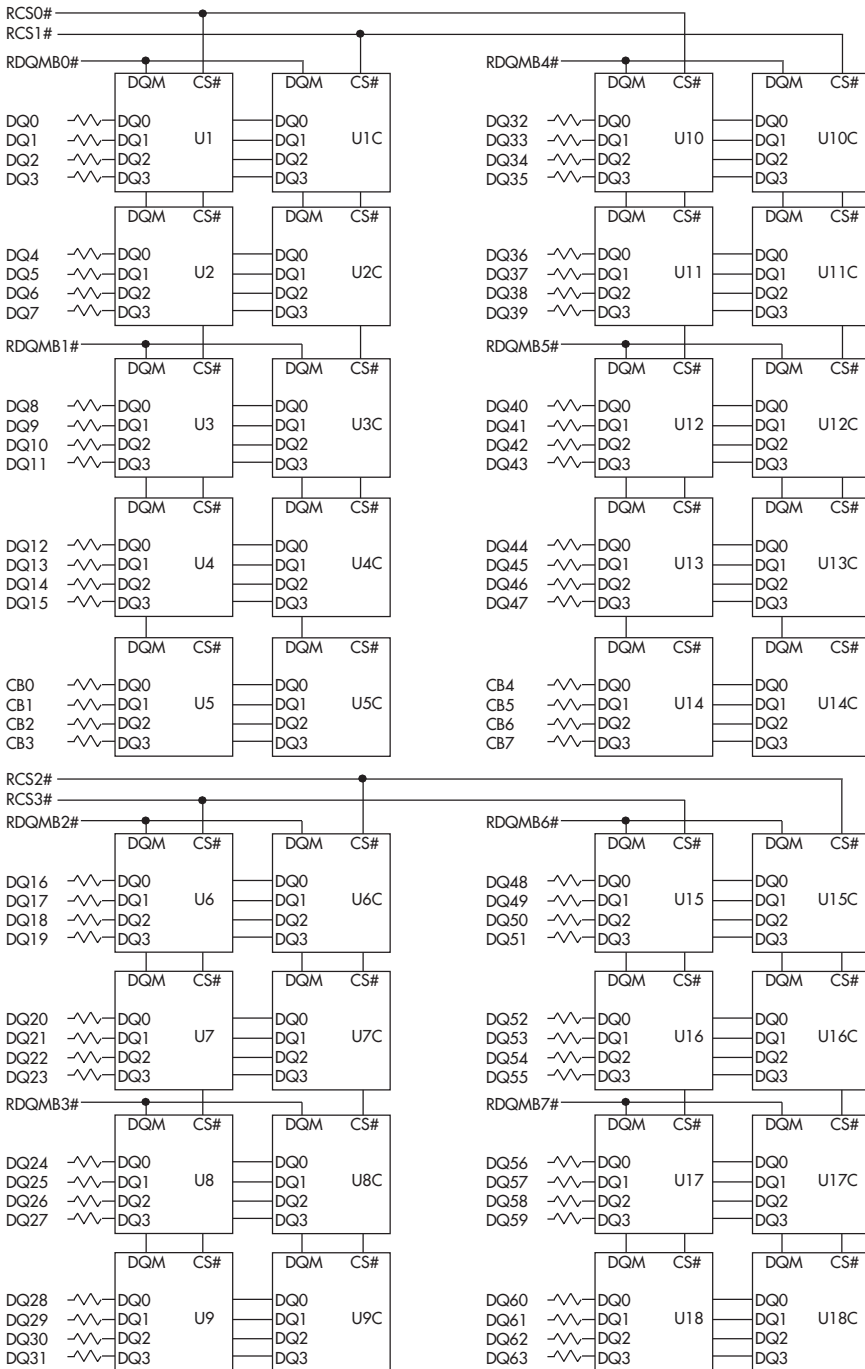


*CKE1 not used on single bank configurations

U1-U18 = 16M x4, 32M x4, or 64M x4 SDRAM TSOP components

16M x72, 32M x72, 64M x72, 128M x72 SDRAM DIMM
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Functional Block Diagram utilizing Canopy™ technology



NOTE:
The standard configuration for this module is to have CKE0 wired to one physical bank, and CKE1 wired to the second physical bank. This design also has the option to have CKE0 wired to all SDRAM's.
U1-U18 = 32M x4 or 64M x4 SDRAM TSOP components
U1C-U18C = 32M x4 or 64M x4 SDRAM TSOP Canopy™ components

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