

# ET3000k10M and ET3000k10S Frequently Asked Questions (FAQ)

(Updated 2/19/03)

**Q: Is it possible to do level conversion to 1.8V & 2.5V?**

Level Conversion can be done by plugging the daughter card into one of the three 200 pin connectors on the ET3000k10/S. A single daughter card can do level translation to a single voltage using a quickswitch or an active buffer.

**Q: Is it possible to control the VCCO of each bank of the FPGA?**

No. We used all of the signals of I/O, so it is not possible to control VCCO on any bank.

**Q: Can I socket any or all of the FPGA's?**

We prefer not to do this – we have yet to find a socket in the 1152FF package that is reliable enough to justify. Also, the price that we would need to charge for a product that has a socket would make most customers fall out of their chairs.

**Q: Can I stack ET3000k10M's or ET3000k10S'?**

No. We eliminated that feature in this product.

**Q: Can I put multiple ET3000k10/S's in the same PC?**

Yes, provided you have a reasonable PCI design in FPGA\_F, you should be able to put as many DN3000k10/S's in the same PCI backplane as will mechanically fit. Be aware, however, that the SDRAM sticks straight out – it isn't angled. So each ET3000k10/S probably needs two PCI slots.

## Note: Warning about Advanced Communication Riser (ACR) Slots



Above is a picture of the Asus A7v266-E motherboard ([7v266-e link](#)). We use this motherboard as the basis for a high performance workstation. We are worried about the slot on the far left of board which ASUS calls an Advanced Communication Riser (ACR) slot. Note that it is a +5V PCI connector installed backwards and offset a little. A +5V PCI connector installed backwards makes a +3.3V PCI slot. If this motherboard is not mounted in a chassis, it is quite easy to plug a +3.3V PCI board into this slot. Please DON'T DO THIS – it is not a +3.3V PCI slot.

**Advanced Communication Riser slot == BAD!**

### Q: What type of PCI slot is needed? What motherboards do you recommend?

The ET3000k10, ET3000k10S, ET2000k10 (with VirtexE), ET3000k10A, and ET3000k10AS are not +5V tolerant since the FPGA's connecting to the PCI bus cannot tolerate +5V signaling. All of our products are mechanically keyed so that you cannot plug the board into the wrong type of slot. Be careful if you are using a motherboard that is not in a chassis. PCI boards that are keyed for +3.3V can be plugged backwards into +5V PCI slots. This is immediately fatal to the board. We prefer you use our products with our PCI extender, the [DNPCIEXT-S3](#). If you want to plug these boards directly into a PCI slot, the motherboard must have a +3.3V PCI slot. The motherboard we use here in La Jolla to test the boards is a SuperMicro 370DLE <[SuperMicro DLE370 motherboard specifications](#)>. This motherboard, however, doesn't have an AGP slot, so a PCI-based video card is necessary. Please note that any PCI-complaint motherboard that has a 66MHz/64-bit PCI slot should work. PCI slots that are 66MHz/64-bits are by definition +3.3V. Remember to add the jumper that grounds M66EN (66MHz Enable) on the board if you want to force the bus to clock the PCI bus at 33MHz.

If you want to get a PC that is identical to the ones we use here, contact Memory Depot [Memory Depot Web Page](#) and tell them you are working with our products. They can build a PC that is identical to the ones that we use without much fanfare.

Note that +3.3V is not needed on the backplane. We generate +3.3V on the board for all of our products.

### **Q: If need to close the case, is this possible?**

The ET3000k10AS is a standard full-sized PCI card and should fit into all standard PCI slots including servers and Sun workstations. The DN3000k10S will fit in all towers that we have seen, but this is not a standard PCI board – it is of AT length, and it is too tall. Sun workstations cannot fit a PCI card of AT length, so unless you repackage your Sun, you will need to use one of our extenders. The ET3000k10 is of AT length, and taller than the ET3000k10. The dimensions are in the [User's Manual](#). We have found an ATX tower from Swiftech that has a deep enough cavity to fit the DN3000k10 and put the lid on. I have a few of these in La Jolla if you want one – I paid \$200. I got three of them at Fry's. The part number is FS020-SM3. I don't have a datasheet, and I cannot find any reference to this tower on the web. I'll post some pictures on our web page as soon as I get a chance.

### **Q: I want to encrypt the bitstream. You disabled this function. What gives?**

We have disabled the encryption function using SelectMap via the SmartMedia card for both the ET3000k10M and ET3000k10S. **Do not use this function.** When using an encrypted bitstream, the JTAG method of configuring seems to be OK. The slower speed of JTAG however may prevent it from being an acceptable alternative. I am writing this in late April of 2002, and as of this date Xilinx hasn't come completely clean on the seriousness of the encryption bugs when using SelectMap. Here is what we have found:

- If a key is loaded and the bitstream related to that key is loaded into a 2v6000, everything is fine and encryption works. We had to slow down the configuration speed significantly to get it to work, but a 2v6000 still configures in seconds (as opposed to minutes or hours).
- If a key is loaded and a bitstream not related to that key is loaded into a 2v6000, the part draws a ton of current – in excess of 5A on +1.5V.
- If the wrong key is loaded, the part draws a ton of current – again in excess of 5A on +1.5V.

The only thing that prevents the part from blowing up on the ET3000k10S is the reset circuit, which detects a drop on the +1.5V supply and resets that board, terminating the configuration process. The ET3000k10 has a 10A supply on +1.5V, and we think this is more than enough power to damage a 2v6000.

Let me summarize the problem with encryption:

***If you don't have exactly the right key and exactly the right bitstream, you smoke your board.***

We think it is perfectly normal to attempt to load a bitstream into a device that may not be related to the key. We also think it is reasonable to load an incorrect key. Neither of these 'mistakes', if you want to call them that, should be fatal. To prevent you from damaging our products, we have disabled the function via

SelectMap. If the processor detects that you are attempting to load a bitstream that has been encrypted, it will refuse the bitstream. Use the RS232 port to get additional feedback from the configuration process. More information can be gotten from the Xilinx White paper, wp155\_03.pdf, which is on our web page.

### **Q: Why am I having problems with my SIIG CF+SM USB Combo reader?**

The SIIG USB reader with part number JU-CFSM22 can only successfully write to the first 64MB of a 128MB Smart Media card. This reader does not seem to have any problems with cards that are smaller than 128MB. Emulation Technology recommends using the SmartDisk FlashPath floppy adapter to read/write to all sizes of Smart Media cards.

### **Q: Why won't the Xilinx tools let me use programming pins as I/O in my design?**

The following programming pins can be used as I/O after configuration is complete: Din/D0, D[7:1], CS\_B, RDWR\_B, BUSY/DOUT, INIT\_B. Other programming pins (PROG\_B, DONE, M[2:0], HSWAP\_EN, PWRDWN\_B) may never be used for I/O.

To allow programming pins to become user I/O after configuration, the "Persistent Pins" option has to be turned off. Xilinx Project Navigator and Design Manager will automatically turn this option off if Readback and Reconfiguration are both disabled, and turn it on otherwise. However, Virtex-II chips will not configure at all if Reconfiguration is disabled.

To work around this, run the Xilinx tools with Readback disabled, but Reconfiguration enabled. After the design is placed and routed, bitgen will give you errors:

```
ERROR:Bitgen:145 - Pin XX## is a persistent pin, but a component exists in it's
```

```
IOB. Please rerun par with the persistent pins prohibited from use.
```

Look in the folder where your design is being created for a file named "bitgen.ut" and open it in a text editor. You should see a line that reads "-g Security:LEVEL1" which indicates that Readback is disabled and Reconfiguration is enabled. You should also see a line that reads "-g Persist:Yes" which you should change to read "Persist:No." Save the file, then open a command prompt window. Change directory to the folder with the design in it, type "bitgen <your design>.ncd -w -f bitgen.ut" and hit enter.

### **Q. I am using Xilinx 4.2i, why is the software creating small bit files?**

You must install service pack 3 for 4.2i to correct this problem.

### **Q: How can I change the addresses used for my Base Address Registers?**

You can't. The BARs are assigned by the PCI BIOS at startup. You can change whether a BAR is Memory or IO space, and you can change it's size, both of which may or may not affect the address it is assigned. If you are having memory conflicts, there may be something wrong with your BIOS, or read the next question:

**Q: PCI accesses to the board fail in Windows 2000. I investigated, and found a memory space conflict between the board and another device. How can I fix this?**

We have found that some Windows systems cannot allocate enough memory to satisfy the reference design. To fix this, the software CD contains an alternate driver, QLDRIVER\_16MB.sys, which restricts each BAR to a maximum of 16 megabytes. This has fixed the problem on most systems; if it does not, editing the reference design to make BAR1 smaller may work.

If PCI accesses still fail, you may have a more serious problem. Check your BIOS settings; if that doesn't help, please test the board under DOS, on the same machine if possible, to see if the problem remains. Then contact The Dini Group for assistance.

**Q: I want to interface your board with a device having differential LVPECL outputs. What is required?**

For every differential pin-pair (Virtex-E and Virtex-II I/Os) being used as an LVPECL receiver, a 100 ohm resistor should be placed across and near the receiver pins. There are no provisions for placing these resistors on our boards.

**Q: I have a DN3000k10 and I want the FPGAs to start-up simultaneously. How I can do this?**

First you need to check what version of the processor/cpld code your board is programmed with. To do this, hook up the RS232 port as described in the section titled "Setting up the Serial Port (J27 – RS232 Port)" on pg 2-21 of the User's Manual. Power up the board and the title for the Main Menu should have a Config\_LIB revision number. If your revision is 1.26 or higher then all you need to do is install a jumper on J17 connecting pins 7 and 8. Please note that in order to bring up the FPGAs simultaneously, you must have the bitgen option DriveDone set to NO. If the revision is less than 1.26 then you will need to download the latest Processor/CPLD update from

[http://www.emulationtechnology.com/catalog/off-the-shelf\\_solutions/3k\\_cpld\\_uP.zip](http://www.emulationtechnology.com/catalog/off-the-shelf_solutions/3k_cpld_uP.zip)

After updating both the CPLD and the processor, install the jumper as described above.

**Q: I have a ET3000k10M and I want the FPGAs to get a reset pulse after they have all been configured. How I can do this?**

First you need to check what version of the processor/cpld code your board is programmed with. To do this, hook up the RS232 port as described in the section titled "Setting up the Serial Port (J27 – RS232 Port)" on pg 2-21 of the User's Manual. Power up the board and the title for the Main Menu should have a Config\_LIB revision number. If your revision is 1.26 or higher then all you need to do is install a jumper

on J17 connecting pins 9 and 10. If the jumper is installed then after all FPGAs have been configured there will be a high pulse on pin AL30. If the revision is less than 1.26 then you will need to download the latest Processor/CPLD update from

[http://www.emulationtechnology.com/catalog/off-the-shelf\\_solutions/3k\\_cpld\\_uP.zip](http://www.emulationtechnology.com/catalog/off-the-shelf_solutions/3k_cpld_uP.zip)

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